We Claim:

1. A method for testing circuits that transmit and/or receive data values via high frequency signals, using only low frequency analog test circuitry, comprising:

a. coupling a transmitter of said signals to a receiver via a capacitance and connecting an input of said receiver to a bias voltage;

b. applying a source of DC current to said receiver input via an impedance;

c. transmitting one or more sequences of different data values while applying one of at least two values of said DC current; and

d. testing received data values.

2. A method according to claim **1**, said applying a source of DC current comprises applying a DC constant current source to the receiver.

3. A method according to claim **1**, said applying a source of DC current comprises applying a DC constant voltage source to the receiver.

4. A method according to claim **1**, said applying a source of DC current includes applying two separate current sources to said receiver when said receiver input is differential.

5. A method according to claim **4**, said applying two separate currents sources includes applying two currents which have substantially equal but opposite values.

6. A method according to claim **4**, said applying two separate current sources includes applying two DC constant voltage sources whose voltage values are equal to the voltage that would be measured at the outputs of said DC constant current sources.

7. A method according to claim **1**, in which said impedance is a resistor.

8. A method according to claim **1**, in which said impedance is an inductor.

9. A method according to claim **1**, further including selecting transmitted data values so as to increase the susceptibility of signals to circuit parameters.

10. A method according to claim **1**, said testing received data values includes measuring bit error rate (BER) of said signals.

11. A method according to claim **1**, further including attenuating the signal level of the transmitted signal relative to its maximum signal level.

12. A method according to claim **11**, said attenuating the signal level including reducing the drive current of the transmitter.

13. A method according to claim **11**, said attenuating the signal level including applying a resistor network between said transmitter and said receiver.

14. A method according to claim **11**, said attenuating the signal level including connecting a load capacitor.

15. A circuit for testing circuits that transmit and/or receive data values via high frequency signals, using only low frequency analog test circuitry, comprising:

a transmitter for transmitting said signals;

a receiver for receiving said signals;

a coupling capacitor connected between said transmitter and said receiver; and

means for generating a variable bias voltage connected to at least one receiver input.

16. A circuit as defined in claim **15**, further including:

means for resistively attenuating signals output by said transmitter;

a load capacitor having a value which causes signal transition times greater than one data unit interval connected between said transmitter and said receiver.

17. A method for testing the circuit of claim **15**, comprising:

adjusting the bias voltage to change the eye-opening of the signal applied to said receiver;

applying data patterns to the circuit that change the eye-opening and bit error rate said signal;

measuring bit error rate for each data pattern and bias voltage; and

comparing the measured bit error rates to test limits to determine whether a circuit under test passes or fails.

18. A method for parametrically testing circuits that transmit and/or receive high frequency data via differential signals using only low frequency test circuitry, comprising:

resistively attenuating a transmitted signal and applying to said signal a load capacitance having a value that causes digital transition times to exceed one unit interval to produce an attenuated signal;

connecting a DC voltage or current to a signal path between a transmitter of said signal and a receiver of said signal; and

testing the bit error rate (BER) of said attenuated signal while altering a DC bias voltage or current applied to said attenuated signal.

19. A method for testing the performance of the input and/or output of a digital circuit, comprising:

attenuating a differential signal applied to or output from said circuit relative to a normal voltage swing of said signal and filtering said signal using a capacitance having a value with a time constant that is comparable to a data bit duration (unit interval) to produce a filtered signal;

AC-coupling said filtered signal to the inputs of a differential receiver whose inputs can be biased to different DC bias voltages;

while monitoring bit error rate (BER) of said signal, adjusting bias voltage to increase or decrease the amplitude of single-ended logic 1's in the filtered signal and adjusting the number of consecutive logic 1's in test patterns used to generate said signal so that said capacitance permits the received edge timing to be adjusted precisely; and

calculating the amplitude of the signal based on measured average voltages of the signal while the percentage and grouping of logic 1's in the signal are adjusted.